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APPLICATION NO.	F	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
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P.O. BOX 2550 SALT LAKE CITY, UT 84110				VIGUSHIN	VIGUSHIN, JOHN B	
				ART UNIT	PAPER NUMBER	
				2827	2827	
				DATE MAILED: 08/07/2003		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)					
	09/916,197	HUI ET AL.					
Office Action Summary	Examiner	Art Unit					
	John B. Vigushin	2827					
The MAILING DATE of this communication app Period for Reply	The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status							
1) Responsive to communication(s) filed on 29 A	pril 2003 .						
2a)⊠ This action is FINAL . 2b)□ Thi	s action is non-final.						
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims							
4)⊠ Claim(s) <u>1-14,16-35,37-56,58-76 and 78-118</u> i	s/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.							
5)⊠ Claim(s) <u>80-98</u> is/are allowed.							
6)⊠ Claim(s) <u>1-14,16,20-35,37-56,60-76,79,99-115 and 118</u> is/are rejected.							
7)⊠ Claim(s) <u>17-19,58,59,78,116 and 117</u> is/are objected to.							
8) Claim(s) are subject to restriction and/or election requirement.							
Application Papers							
9)☐ The specification is objected to by the Examiner.							
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
11)⊠ The proposed drawing correction filed on <u>29 April 2003</u> is: a)⊠ approved b)⊡ disapproved by the Examiner.							
If approved, corrected drawings are required in reply to this Office action.							
12)☐ The oath or declaration is objected to by the Examiner.							
Priority under 35 U.S.C. §§ 119 and 120							
13)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a)⊠ All b)☐ Some * c)☐ None of:							
1.⊠ Certified copies of the priority documents have been received.							
Certified copies of the priority documents	have been received in Application	on No					
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.							
14) ☐ Acknowledgment is made of a claim for domestic	priority under 35 U.S.C. § 119(e	e) (to a provisional application).					
a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.							
Attachment(s)							
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 020	5) Notice of Informal F	(PTO-413) Paper No(s) Patent Application (PTO-152)					
J.S. Patent and Trademark Office PTO-326 (Rev. 04-01) Office Acti	on Summary	Part of Paper No. 0801					

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed April 29, 2003 (Certificate of Mailing date: April 25, 2003). The Examiner acknowledges the amendments to Claims 1, 16, 17, 19, 21, 37, 39, 41, 58, 63, 78 and 79, the cancellation of Claims 15, 36, 57 and 77, and the addition of Claims 80-118. Claims 1-14, 16-35, 37-56, 58-76 and 78-118 are now pending in the instant amended Application.

Claim Rejections - 35 USC § 112

- The following is a quotation of the second paragraph of 35 U.S.C. 112:
 The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 3. Claims 99-115 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 99 recites, in the last three lines of the claim, "contact pads **exposed to** a surface of said substrate element adjacent to which said coverlay is positioned being exposed through or beyond an outer periphery of said coverlay." (Bold emphasis added). There is no support in Applicant's disclosure for, or any structural sense in "contact pads **exposed to** a surface of said substrate...." The rejection may be easily overcome by replacing "**exposed to**" with **--on--**.

Claims 100-115 depend from the above rejected Claim 99 and therefore inherit the defect of the claim.

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Rejections Based On Prior Art

4. The following references were relied upon for the rejections hereinbelow:

Takehara (US 6,476,507 B1)*

Sasaki (US 6,175,159 B1)*

Toh et al. (US 6,091,140)*

Eng et al. (US 6,087,203)*

Farnworth et al. (US 6,020,629)*

*Already made of record in the instant Application.

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 1, 2, 6, 7, 9, 10, 16 and 20 are rejected under 35 U.S.C. 103(a) as obvious over Takehara alone or, in the alternative, in view of Sasaki.
 - A1) Rejection #1 (over Takehara alone):
- la. Takehara discloses, in Figs. 1, 2 and 6: a semiconductor die (1, 21) with a plurality of bond pads arranged on an active surface thereof (col.7: 18-21); a tape (2, 29) positioned over the active surface, the tape 29 including at least one slot (corresponding to substrate openings 12, 22; col.7: 55-60; col.11: 43-45) formed therethrough, each of the plurality of bond pads being exposed through the at least one slot, at least one end of the at least one slot extending beyond an outer periphery of semiconductor die (1, 21) (col.11: 43-45); a substrate element (3, 19) positioned over

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tape (2, 29) opposite semiconductor die (1, 21), the substrate element (3, 19) including a plurality of contact areas, each contact area of the plurality corresponding to a bond pad of the plurality of bond pads and electrically connected thereto by way of an intermediate conductive element--i.e., bonding wire (4, 30)--that extends through at least one opening (12, 22; col.7: 55-60; col.11: 50-53) formed through the substrate element (3, 19) and aligned with the at least one slot of tape (2, 29) (Fig. 6; col.7: 18-21; col.11: 10-13 and 43-45), substrate element (3, 19) further including a contact pad 5 in communication with each contact area of the plurality of contact areas by way of a substantially laterally extending conductive trace in the substrate (col.7: 21-24) {Examiner's Note: col.7: 21-22 recite "[i]n the substrate 3, the wire electrically connects the pad with an external terminal 5..." (bold emphasis by the Examiner). The Examiner takes the position that "the wire" in the substrate is not referencing the bonding wire 4; rather "the wire" in, or a part of, the substrate is a trace (not shown), distinct from bonding wire 4. Furthermore "the pad" in the above-cited col.7: 21-22 is referring to "a pad (not shown) of the substrate 3" cited in col.7; 20-21 and not "a pad (not shown) of the semiconductor chip 1" cited in col.7: 19-20 because 'the wire"--i.e., trace—in the substrate connects "the pad (not shown)" of the substrate to the terminal 5 of the substrate. Takehara does not provide any solid evidence of electrically connecting the contact bonding area of the substrate to the substrate terminal 5 with bonding wire 4 (e.g., none of the Drawings show such a construction and it is not entirely clear whether "the wire" in col.7: 19-20 is one and the same as bonding wire 4). Furthermore, the terminal 5 is configured to receive solder bump 6, and not configured

to additionally receive a bonding wire 4. Therefore, the connection between the substrate terminal 5 and substrate wire-bond pad is evidently a "wire" in or on the circuit substrate 3; i.e., a trace); a quantity of encapsulant material (7, 28) substantially filling a volume defined by the at least one slot (corresponding to substrate openings 12, 22; col.11: 43-45) of tape (2, 29) and the at least one opening (12, 22) of the substrate element (3, 19).

A2) Rejection #2 (over Takehara in view of Sasaki):

Ib. Takehara discloses, in Figs. 1, 2 and 6: a semiconductor die (1, 21) with a plurality of bond pads arranged on an active surface thereof (col.7: 18-21); a tape (2, 29) positioned over the active surface, the tape 29 including at least one slot (corresponding to substrate openings 12, 22; col.7: 55-60; col.11: 43-45) formed therethrough, each of the plurality of bond pads being exposed through the at least one slot, at least one end of the at least one slot extending beyond an outer periphery of semiconductor die (1, 21) (col.11: 43-45); a substrate element (3, 19) positioned over tape (2, 29) opposite semiconductor die (1, 21), the substrate element (3, 19) including a plurality of contact areas, each contact area of the plurality corresponding to a bond pad of the plurality of bond pads and electrically connected thereto by way of an intermediate conductive element--i.e., bonding wire (4, 30)--that extends through at least one opening (12, 22; col.7: 55-60; col.11: 50-53) formed through the substrate element (3, 19) and aligned with the at least one slot of tape (2, 29) (Fig. 6; col.7: 18-21; col.11: 10-13 and 43-45), substrate element (3, 19) further including a contact pad 5 in communication with each contact area of the plurality of contact areas by way of a

"wire" (col.7: 21-24); i.e., "[i]n the substrate 3, the wire electrically connects the [substrate] pad with an external terminal 5, on which a solder bump 6....is provided" (col.7: 21-23).

IIa. Takehara does not discuss in the disclosure, or show in the drawings, how a "wire" such as bonding wire 4 is to be connected from the substrate wire-bonding contact area pad to the terminal pad 5 when the terminal pad 5 already has a solder bump 6 mounted thereon. Takehara also does not explicitly disclose a substantially laterally extending conductive trace connecting the substrate wire-bonding contact area to the solder-bumped terminal pad 5.

IIb. Sasaki discloses a carrier/interposer substrate 33 that mounts a semiconductor die 32 wherein bond wires 39 connect die 32 to wire-bonding pads 34a (i.e., contact areas) on substrate 33, and wire-bonding pads 34a are connected to external contact pads 34b (having solder balls 40 mounted thereon) by substantially laterally extending traces 34 (Figs. 1, 2A and 2B; col.5: 38-41 and 44-46).

IIc. Since Takehara and Sasaki are in the same semiconductor packaging art and since Takehara refers to the wire "in the substrate 3" as "the wire" (Takehara, col.7: 21-22) and does not specifically and clearly identify it as one and the same as bonding wire 4 (bonding wire 4 clearly being an art-recognized bonding wire), and since it is not likely or evidently practical that the bonding wire 4 would also be wire-bonded to an external contact pad 5 which already has a solder bump 6 attached thereto, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, in the carrier/interposer substrate of Takehara, the practical connection

scheme between wire-bonding contact areas and external connection contact pads on the carrier/interposer substrate taught by Sasaki, wherein the wire-bonding contact areas are connected to solder-bumped external connection contact pads by means of substantially laterally extending **traces**. For even if Takehara actually contemplated the above-mentioned "wire" (see quote of the reference passage in section I, above) as a bonding wire (like bonding wire 4 in Fig. 1) for connecting the substrate wire-bonding contact area to the substrate solder-bumped external connection contact pad 5, such a "bonding wire" connection could easily become shorted with a neighboring bonding wire, which does not happen between traces printed/plated on, or in, the substrate, and the traces of Sasaki can be better configured and dimensioned to both enable a higher density circuit layout on the substrate than can be achieved by bonding wires and avoid the parasitic induction effects common to looped bonding wire connections.

Illa. Further to <u>Rejection #1</u> and <u>Rejection #2</u>, above, Takehara discloses, in Figs. 2 and 3, a coverlay 10 positioned on a surface of the substrate element 9 opposite tape 2, the coverlay substantially covering at least the at least one opening 12 through the substrate element 9 during the injection molding process (col.7: 54-col.8: 51) and removed upon completion of the encapsulation (col.8: 52-54). However, Takehara is silent as to how the coverlay 10 is maintained on the surface of substrate element 9 during the injection molding process and whether the means by which this is accomplished would constitute a "securing" of the coverlay to the surface of substrate 9.

IIIb. Now it is old and well-known in the art that coverlays (i.e., molds) are held in place during the injection molding process by biasing the coverlays (molds) against the

substrate, as indicated by the Applicant (see p.19 of the above-cited instant Amendment, second paragraph). Also, in one molding process embodiment of Takehara, coverlay 10 and coverlay 11 are held in place on the substrate by vacuum induced pressure (col.12: 15-25). By means of the vacuum or other old and well-known types of biasing means (external pressure jig, clamps, etc.), the Examiner takes the position that the coverlays (molds) 10 and 11 are *inherently* "secured" to the substrate; i.e., "secured" in the sense that they are held in place such that they are prevented from moving or slipping out of position by the biasing means (external pressure jig, clamps, vacuum, etc.) for the duration of the molding process.

Illc. Since coverlays (molds) 10 and 11 are used to effect the encapsulation in Takehara by an injection molding process (Figs. 2 and 3, and col.7: 54-8: 54), and holding in place of the coverlays for at least the duration of the molding process would have been readily recognized as beneficial to reliability of the disclosed molding process in Takehara, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide any known convenient biasing means (e.g., external pressure jig, clamps, vacuum, etc.) on the coverlay 10 (and the coverlay 11) of Takehara for the duration of the injection molding process in order to keep the coverlay 10 (and the coverlay 11) secured to the substrate 9 after positioning, i.e., preventing the coverlay 10 (and the coverlay 11) from slipping out of position during the injection molding process with the added benefit of an easy coverlay removal step (i.e., by means of a simple release or removal of the biasing means) after the injection process is completed.

B) Claims 2, 6, 7, 9, 10, 16 and 20 are rejected over modified Takehara as set forth in section 6, pp.14-15 of the previous Office Action of February 04, 2003.

- 7. Claims 5, 25, 27 and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takehara (regarding Claims 5, 25, 27 and 69), or, in the alternative, Takehara in view of Sasaki (regarding Claim 5), as set forth in section 7, pp.15-16 of the previous Office Action of February 04, 2003.
- 8. Claims 8 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takehara (regarding Claims 8 and 44), as applied to Claims 1 and 41-43, above, or, in the alternative, Takehara in view of Sasaki (regarding Claim 8), as applied to Claim 1, above, and further in view of Toh et al. and Farnworth et al., as set forth in section 8, pp.16-19 of the previous Office Action of February 04, 2003.
- 9. Claims 3, 4, 11-14, 23, 24, 29-32, 42, 43, 49, 50, 67, 68 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takehara in view of Eng et al. (regarding Claims 3, 4, 11-14, 23, 24, 29-32, 42, 43, 49, 50, 67, 68 and 72), or, in the alternative, Takehara in view of Sasaki, as applied to Claim 1, above, and further in view of Eng et al. (regarding Claims 3, 4 and 11-14), as set forth in section 9, pp.19-26 of the previous Office Action of February 04, 2003.
- 10. Claims 21, 22, 26, 28, 33-35, 37-41, 45-48, 51-56, 60-66, 70, 71, 73-76, 79 and 118 are rejected under 35 U.S.C. 103(a) as obvious over Takehara.

A) As to Claim 21:

I. Takehara discloses, in Figs. 1-3 and 6: a semiconductor die (1, 21) with at least one bond pad on an active surface thereof (col.7: 18-21); a tape (2, 29) secured to

the active surface, the tape (2, 29) including a slot (corresponding to substrate openings 12, 22; col.7: 55-60; col.11: 43-45) formed therethrough with at least one bond pad being exposed through the slot (Figs. 1 and 6), at least one end of the slot extending beyond an outer periphery of the semiconductor die (1, 21) (col.11: 43-45); and a substrate element (3, 9, 19) positioned over semiconductor die (1, 21) opposite the tape (2, 29) from the semiconductor die (1, 21), the substrate element (3, 9, 19) including at least one opening (12, 22) formed therethrough through which the at least one bond pad is exposed (Figs. 1 and 6).

- II. Takehara further discloses, in Figs. 2 and 3, a coverlay 10 positioned on a surface of the substrate element 9 opposite tape 2, the coverlay substantially covering at least the at least one opening 12 through the substrate element 9 during the injection molding process (col.7: 54-col.8: 51) and removed upon completion of the encapsulation (col.8: 52-54). However, Takehara is silent as to how the coverlay 10 is maintained on the surface of substrate element 9 during the injection molding process and whether the means by which this is accomplished would constitute a "securing" of the coverlay to the surface of substrate 9.
- III. Now it is old and well-known in the art that coverlays (i.e., molds) are held in place during the injection molding process by biasing the coverlays (molds) against the substrate, as indicated by the Applicant (see p.19 of the above-cited instant Amendment, second paragraph). Also, in one molding process embodiment of Takehara, coverlay 10 and coverlay 11 are held in place on the substrate by vacuum induced pressure (col.12: 15-25). By means of the vacuum or other old and well-known

types of biasing means (external pressure jig, clamps, etc.), the Examiner takes the position that the coverlays (molds) 10 and 11 are *inherently* "secured" to the substrate; i.e., "secured" in the sense that they are held in place such that they are prevented from moving or slipping out of position by the biasing means (external pressure jig, clamps, vacuum, etc.) for the duration of the molding process.

IV. Since coverlays (molds) 10 and 11 are used to effect the encapsulation in Takehara by an injection molding process (Figs. 2 and 3, and col.7: 54-8: 54), and holding in place of the coverlays for at least the duration of the molding process would have been readily recognized as beneficial to reliability of the disclosed molding process in Takehara, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide any convenient biasing means (e.g., external pressure jig, clamps, vacuum, etc.) on the coverlay 10 (and the coverlay 11) of Takehara for the duration of the injection molding process in order to keep the coverlay 10 (and the coverlay 11) secured to the substrate 9 after positioning, i.e., preventing the coverlay 10 (and the coverlay 11) from slipping out of position during the injection molding process with the added benefit of an easy coverlay removal step (i.e., by means of a simple release or removal of the biasing means) after the injection process is completed.

B) Claims 22, 26, 28, 33-35 and 37-40 are rejected over modified Takehara as set forth in section 4, pp.3-5 of the previous Office Action of February 04, 2003.

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C) As to Claim 118, modified Takehara further discloses that coverlay 10 is removably secured to the surface of substrate element 9 (removed upon completion of the molding process; col.8: 52-54).

D) As to Claim 41:

I. Takehara discloses, in Figs. 1 and 6: positioning a tape (2, 29) over the active surface of a semiconductor die (1, 21) so that the at least one bond pad on the at least one bond pad on the active surface is exposed through a slot (corresponding to opening 12, 22 in the substrate element 3, 19) formed through tape (2, 29) and at least one end of the slot extends beyond an outer periphery of semiconductor die (1, 21) (col.11: 43-45); positioning a substrate element (3, 19) over tape (2, 29) so that at least one bond pad is exposed through at least one opening (12, 22) formed through substrate element (3, 19) and aligned with the slot (col.11: 43-49), the substrate element (3, 19) including at least one contact area (to which at least one bond wire 4, 30 is connected) corresponding to the at least one die bond pad (col.7: 18-21; col.11: 8-13); electrically connecting at least one bond pad to the at least one contact area (Fig. 1); positioning a coverlay 10 on an exposed surface of substrate element 9 (Figs. 2 and 3) to substantially cover the at least one opening (12, 22) formed through substrate element (3, 9, 19) (Figs. 1-3 and 6; col.7: 54-60); introducing encapsulant material 7 through at least one end into a receptacle formed by the coverlay 10, the at least one opening (12, 22), the slot, and the semiconductor die (1, 21) from a location opposite the semiconductor die (1, 21) from tape (2, 29) (Fig. 3; col.8: 13-19).

II. Takehara, as stated in part I., above, discloses that the coverlay 10 is positioned on an exposed surface of substrate element 9 (Figs. 2 and 3) to substantially cover the at least one opening (12, 22) formed through substrate element (3, 9, 19) (Figs. 1-3 and 6; col.7: 54-60) and further discloses that coverlay 10 is removed upon completion of the encapsulation (col.8: 52-54). However, Takehara is silent as to how the coverlay 10 is maintained on the surface of substrate element 9 during the injection molding process and whether the means by which this is accomplished would constitute a "securing" of the coverlay to the surface of substrate 9.

III. Now it is old and well-known in the art that coverlays (i.e., molds) are held in place during the injection molding process by biasing the coverlays (molds) against the substrate, as indicated by the Applicant (see p.19 of the above-cited instant Amendment, second paragraph). Also, in one molding process embodiment of Takehara, coverlay 10 and coverlay 11 are held in place on the substrate by vacuum induced pressure (col.12: 15-25). By means of the vacuum or other old and well-known types of biasing means (external pressure jig, clamps, etc.), the Examiner takes the position that the coverlays (molds) 10 and 11 are *inherently* "secured" to the substrate; i.e., "secured" in the sense that they are held in place such that they are prevented from moving or slipping out of position by the biasing means (external pressure jig, clamps, vacuum, etc.) for the duration of the molding process.

IV. Since coverlays (molds) 10 and 11 are used to effect the encapsulation in Takehara by an injection molding process (Figs. 2 and 3, and col.7: 54-8: 54), and holding in place of the coverlays for at least the duration of the molding process would

have been readily recognized in Takehara as beneficial to the reliability of the disclosed molding process, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide any convenient biasing means (e.g., external pressure jig, clamps, vacuum, etc.) on the coverlay 10 (and the coverlay 11) for the duration of the injection molding process in order to keep the coverlay 10 (and the coverlay 11) **secured** to the substrate 9 after positioning, i.e., preventing the coverlay 10 (and the coverlay 11) from slipping out of position during the injection molding process with the added benefit of an easy coverlay removal step (i.e., by means of a simple release or removal of the biasing means) after the injection process is completed.

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- E) Claims 45-48, 51-56 and 60-62 are rejected over modified Takehara as set forth in section 4, pp.6-7 of the previous Office Action of February 04, 2003.
 - F) As to Claim 63:
- I. Takehara discloses, in Figs. 1-3 and 6: positioning a tape (2, 29) over at least an active surface of a semiconductor die (1, 21), the tape (2, 29) including a slot (corresponding to substrate opening 12, 22) through which at least one bond pad on the active surface of the semiconductor die (1, 21) is exposed, at least a portion of the slot extending laterally beyond an outer periphery of semiconductor die (1, 21) (col.11: 43-45); positioning a substrate element (3, 9, 19) over tape (2, 29) with at least one opening (12, 22) formed through the substrate element (3, 9, 19) being located at least partially over the slot (Fig. 6); positioning a coverlay 10 over substrate element 9 to

substantially seal the at least one opening 12, the coverlay 10 and lateral edges of at least one opening and the slot forming a receptacle (Figs. 2 and 3).

- II. Takehara, as stated in part I., above, discloses that the coverlay 10 is positioned over substrate element 9 to substantially seal the at least one opening 12 (Figs. 2 and 3) and further discloses that coverlay 10 is removed upon completion of the encapsulation (col.8: 52-54). However, Takehara is silent as to how the coverlay 10 is maintained on the surface of substrate element 9 during the injection molding process and whether the means by which this is accomplished would constitute a "securing" of the coverlay to the surface of substrate 9.
- III. Now it is old and well-known in the art that coverlays (i.e., molds) are held in place during the injection molding process by biasing the coverlays (molds) against the substrate, as indicated by the Applicant (see p.19 of the above-cited instant Amendment, second paragraph). Also, in one molding process embodiment of Takehara, coverlay 10 and coverlay 11 are held in place on the substrate by vacuum induced pressure (col.12: 15-25). By means of the vacuum or other old and well-known types of biasing means (external pressure jig, clamps, etc.), the Examiner takes the position that the molds are *inherently* "secured" to the substrate; i.e., "secured" in the sense that they are held in place such that they are prevented from moving or slipping out of position by the biasing means (external pressure jig, clamps, vacuum, etc.) for the duration of the molding process.
- IV. Since coverlays (molds) 10 and 11 are used to effect the encapsulation in Takehara by an injection molding process (Figs. 2 and 3, and col.7: 54-8: 54), and since

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holding in place of the coverlays after the step of positioning for at least the duration of the molding process would have been readily recognized as beneficial to the reliability of the disclosed molding process, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide any convenient biasing means (e.g., external pressure jig, clamps, vacuum, etc.) on the coverlay 10 (and the coverlay 11) for the duration of the injection molding process in order to keep the coverlay 10 (and the coverlay 11) secured to the substrate 9 after positioning, i.e., preventing the coverlay 10 (and the coverlay 11) from slipping out of position during the injection molding process with the added benefit of an easy coverlay removal step (i.e., by means of a simple release or removal of the biasing means) after the injection process is completed.

G) Claims 64-66, 70, 71, 73-76 and 79 are rejected over modified Takehara as set forth in section 4, pp.8-9 of the previous Office Action of February 04, 2003.

Allowable Subject Matter

- 11. Claims 80-98 have been allowed.
- 12. Claims 99-115 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.
- 13. Claims 17-18, 19, 58-59, 78 and 116-117 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 17-18, patentability resides in the limitation wherein *the coverlay is* secured to the substrate element with an adhesive material, in combination with the other limitations of the broadest claim, Claim 17.

As to Claim 19, patentability resides in the limitation wherein contact pads of the substrate element are exposed through or beyond the coverlay, in combination with the other limitations of the claim.

As to Claims 58-59, patentability resides in securing the coverlay to the substrate element with a pressure sensitive adhesive, in combination with the other limitations of the broadest claim, Claim 58.

As to Claim 78, patentability resides in *adhesively securing the coverlay to the* substrate element, in combination with the other limitations of the claim.

As to Claims 80-98, patentability resides in *contact pads of the substrate element* being exposed through or beyond the coverlay, in combination with the other limitations of base Claim 80.

As to Claims 99-115, patentability resides in contact pads on a surface of the substrate element adjacent to which the coverlay is positioned being exposed through or beyond an outer periphery of the coverlay, in combination with the other limitations of base Claim 99.

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As to Claims 116-117, patentability resides in the limitation wherein the coverlay is secured to the surface of the substrate with an adhesive material, in combination with the other limitations of the broadest claim, Claim 116.

15. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Response to Arguments

16. Applicant's arguments filed in the instant Amendment of April 29, 2003 have been fully considered but they are not persuasive.

The Examiner is in full agreement with the Applicant that biasing molds to a substrate in a molding process is well-known in the art and that molds 10 and 11 of Takehara are biased against the substrate in order to hold the assembly in place therefor (see Amendment, p.19, second paragraph). However, the Examiner respectfully disagrees with the Applicant on two important points:

1) Firstly, the coverlay of the Applicant's invention is as much a removable structural part of the molding or encapsulation process, as are upper mold 10 and lower mold 11 of Takehara (compare the encapsulation process of Takehara relied upon for the rejections, above, with the that of the Applicant's invention as discussed in Applicant's Specification, paragraphs [0048] and [0050]). The Applicant does not claim any structural details of the coverlay that would distinguish over those of the upper mold 10 or the lower mold 11 of Takehara. Since the coverlay of the Applicant's invention and

the molds 10 and 11 of Takehara are both removable means for effecting an encapsulation of a semiconductor package, and since the "comprising" language of the claims does not absolutely limit the number of structural elements in the prior art to the number of structural elements in the claims, the Examiner therefore takes the position that upper mold 10 of Takehara reads perfectly on the coverlay of the Applicant's claims, as rejected, above.

2) Secondly, the Examiner takes the position that biasing the coverlay/mold 10, and the coverlay/mold 11, to the surface of the substrate in order to hold them in place on the substrate surface in fact renders the coverlay(s) secured to the surface of the substrate in the sense that the coverlay 10 and coverlay 11 are held in place on the substrate such that they are prevented from moving or slipping out of position by the biasing means (external pressure jig, clamps, vacuum, etc.) for the duration of the molding process. The Examiner takes the position that biasing the coverlay(s) to the substrate in the manner described above results in a structure with a coverlay that is encompassed by the general concept of "securing" or "secured." What the Examiner concedes as evidently allowable over the prior art of record is securing the coverlay to the substrate element with an <u>adhesive</u>, as previously indicated in the Examiner's First Office Action of February 04, 2003 (see p.27, section 11). The Applicant and the Examiner apparently differ over the general concept of "securing" and "secured," hence, in the Applicant's amendment of Claims 1, 21, 41 and 63, the Applicant evidently chose not to amend Claims 1, 21, 41 and 63 with the above-mentioned subject matter previously indicated as allowable over the prior art of record.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chung et al. (US 6,207,478 B1; already made of record in Applicant's IDS filed February 24, 2003) discloses all the limitations of many of the claims of the instant Application including the limitation wherein the contact pads 22 of the substrate element 25 are exposed through or beyond the coverlay 50 (Figs. 10 and 11; col.5: 31-36 and 48-53) but does not teach or suggest at least one end of slot 26a (of tape 26) extending beyond an outer periphery of semiconductor die 21 (Fig. 7).

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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19. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to John B. Vigushin whose telephone number is 703-308-

1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7382

for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is 703-308-

0956.

John B. Vigushin Primary Examiner

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ibv

August 2, 2003